Terms used: **logic cone equivalence fpga dsp** Found **11,807** of **209,709**

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21 CAD for FPGAs: Multiplexer restructuring for FPGA implementation cost reduction

Paul Metzgen, Dominic Nancekievill
June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**
Publisher: ACM Press
Full text available: pdf(691.28 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a novel synthesis algorithm that reduces the area needed for implementing multiplexers on an FPGA by an average of 18%. This is achieved by reducing the number of Lookup Tables (LUTs) needed to implement multiplexers. The algorithm relies on reimplementing 2:1 multiplexer trees using efficient 4:1 multiplexers. The key to the algorithm's performance lies in exploiting the observation that most multiplexers occur in busses. New optimizations are employed which pay a small cost ...

Keywords: FPGA, busses, logic optimization, multiplexers, recoding, restructuring, synthesis

22 Generation of very large circuits to benchmark the partitioning of FPGA

Joachim Pistorius, Edmée Legai, Michel Minoux
April 1999 **Proceedings of the 1999 international symposium on Physical design ISPD '99**
Publisher: ACM Press
Full text available: pdf(1.01 MB) Additional Information: full citation, references, index terms

23 Restructuring logic representations with easily detectable simple disjunctive decompositions

H. Sawada, S. Yamashita, A. Nagoya
February 1998 **Proceedings of the conference on Design, automation and test in Europe DATE '98**
Publisher: IEEE Computer Society
Full text available: pdf(125.30 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Simple disjunctive decomposition is a special case of logic function decompositions, where variables are divided into two disjoint sets and there is only one newly introduced variable. This paper presents that many simple disjunctive decompositions can be found

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FPGA implementation of FIR filters using pipelined bit-serialcanonical signed digit multipliers
S He, M Torkelson - Custom Integrated Circuits Conference, 1994., Proceedings of ..., 1994 - ieeexplore.ieee.org
... addition, outperformances some dedicated commercial **DSP** chips ... can produce a near **equivalent** performance ... in wordlength latency with maximum **logic** level **equivalent** ...
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MA Wickert, J Papenfuss - Microwave Theory and Techniques, IEEE Transactions on, 2001 - ieeexplore.ieee.org
... an asymmetric FIR filter, while introducing the **equivalent** group delay ... with a maximum of 80 000 **logic** gates. ... The **DSP** has enough available bandwidth to easily ...
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A flexible multiplication unit for an **FPGA logic** block - all 3 versions »
K Rajagopalan, P Sutton - Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE ..., 2001 - ieeexplore.ieee.org
... including digital filters, correlators and other **DSP** applications ... architecture requires 3.6 times fewer **logic** blocks (2.8 times fewer **equivalent** gates) than ...
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Programmable **logic** device for real time video processing - all 3 versions »
B Taylor - US Patent 5,857,109, 1999 - Google Patents

Terms used: **technology mapping load clear** Found **77,112** of **209,709**

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21 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(17.07 MB) Additional Information: full citation, abstract, citings

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

22 Logic synthesis and mapping: Placement-driven technology mapping for LUT-based FPGAs

Joey Y. Lin, Ashok Jagannathan, Jason Cong
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: pdf(252.89 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we study the problem of placement-driven technology mapping for table-lookup based FPGA architectures to optimize circuit performance. Early work on technology mapping for FPGAs such as Chortle-d[14] and Flowmap[3] aim to optimize the depth of the mapped solution without consideration of interconnect delay. Later works such as Flowmap-d[7], Bias-Clus[4] and EdgeMap consider interconnect delays during mapping, but do not take into consideration the effects of their mapping solution ...

Keywords: FPGA synthesis, logic re-synthesis, mapping

23 Real-time shading

Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(7.39 MB) Additional Information: full citation, abstract

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S3	8	altera.as. and (logic near3 cones)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:12
S4	20	altera and (logic near3 cones)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:49
S5	35	altera and (technology near3 map)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 13:56
S6	1	("6990650").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/08/26 14:15
S7	24	(technology near3 map) and fpga and dsp	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 14:16
S8	5	(technology near3 map) and fpga and dsp and ((ip or dsp) near3 block)	US-PGPUB; USPAT; USOCR	ADJ	ON	2007/08/26 14:16